REMARKS

Claims 24 - 35 stand rejected under 35 U.S.C. §103 based on U.S. Patent 5,557,764 issued to Stewart et al. ("Stewart") in view of U.S. Patent No. 5,903,749 issued to Kenner et al. ("Kenner"). Claims 24 and 30 are amended.

Stewart discloses:

> An apparatus is provided for processing a plurality of interrupts in a processor system, comprising a plurality of interrupt vector registers each having an interrupt trigger input, each of the interrupt vector registers containing a programmable interrupt vector. A multiplexer is connected to the interrupt-vector-registers-and control logic controls the multiplexer to select one of the interrupt vectors as the selected interrupt vector upon activation of the corresponding interrupt trigger. A slot memory address counter receives the selected interrupt vector through the multiplexer, the slot memory address being controlled by the control logic to load the selected interrupt vector.

(Col. 2, lines 5-17).

Stewart clearly discloses that "A slot memory address counter receives the selected interrupt vector through the multiplexer, the slot memory address being controlled by the control logic to load the selected interrupt vector."

In contrast, claim 24 as amended recites "said selector causing the processor to receive the next program instruction when the master interrupt signal is not asserted, and to receive an interrupt vector directly from the interrupt vector store when the master interrupt signal is asserted," which is neither disclosed nor suggested by Stewart.

Kenner discloses:

> On certain processors (e.g., superscalar processors, very long instruction word processors, etc.), allowing the compiler to reorder the object code instructions can improve performance by exposing simultaneously executable instructions.

(Col. 1, lines 20 - 24). Kenner also discloses:

> Any number of different mechanisms can be used to causes a processor to branch or reload depending on whether a memory conflict was detected. For example, in one embodiment of a processor that supports opcodes, the opcodes for the branch and preload instructions include a bit that indicates if the opcode is valid or invalid. As the instruction progresses through the processor's execution stream, the bit in the opcode can be altered to validate and/or invalidate the opcode. An invalid opcode is not executed. Upon receiving a check no-invalidate branch instruction, a branch instruction whose execution will cause the processor to branch to the label specified in the check no-invalidate branch instruction is inserted into the processor's execution stream. Depending on whether a memory conflict is detected for the check no-invalidate branch instruction, the validity bit in the branch instruction's opcode is altered accordingly. The same approach used for the check no-invalidate branch instruction can be used for the check no-invalidate reload instruction. Thus, upon receiving a check no-invalidate reload instruction, a preload instruction whose execution will cause the processor to reload the data at the data address specified in the check no-invalidate reload instruction is inserted into the processor's execution stream.

(Col. 12, lines 26 - 46).

In contrast, claim 24 as amended recites "said selector causing the processor to receive the next program instruction when the master interrupt signal is not asserted, and to receive an interrupt vector directly from the interrupt vector store when the master interrupt signal is asserted," which is neither disclosed nor suggested by Kenner.

Even if Stewart and Kenner were combined, the combination would neither teach nor suggest "said selector causing the processor to receive the next program instruction when the master interrupt signal is not asserted, and to receive an interrupt vector directly from the interrupt vector store when the master interrupt signal is asserted," as recited in claim 24 as amended.

Therefore, the applicant submits that Claim 24 as amended is patentable over Stewart in view of Kenner. Given that claims 25 - 29 depend from claim 24 as amended, applicant submits that these claims are also patentable over Stewart in view of Kenner.

Claim 30 as amended recites "causing the processor to receive an interrupt vector directly from the interrupt vector store when the master interrupt signal is asserted," which is neither disclosed nor suggested by Stewart and Kenner, either alone or in combination. Therefore, applicant submits that claim 30 as amended is patentable over Stewart in view of Kenner. Given that claims 31-35 depend from claim 30 as amended, applicant submits that these claims are also patentable over Stewart in view of Kenner.

CONCLUSION

Allowance of the claims is respectfully requested. The Examiner may call the Assignee's attorney at (650) 849-4422 to further advance prosecution of this case to issuance.

If the Commissioner determines that additional fees are due or that an excess fee has been paid, the Patent Office is authorized to debit or credit (respectively) Deposit Account No. **50-2518**, referencing billing no. **CA7010642001**.

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